High Efficiency Amplifier Using Rectangular Waveform

Sachihiro Toyoda
Department of Electrical Engineering
Osaka Institute of Technology
5-16-1 Ohmiya, Asahi-ku, Osaka 535, Japan.

Abstract

This paper describes a new high efficiency amplifier. It consists of two circuits: the first one produces the rectangular waveform, and the second one makes its operating angle (current flowing angle) small. Using this waveform with small operating angle, we can obtain an amplifier having large power added efficiency. A single power amplifier using the rectangular waveform was constructed and tested. In the experiment, the operating frequency was in the 0.9 GHz band. The maximum power was 5.1 W, and the power added efficiency was 65 % and 76 % when the operating angle was 70° and 30° , respectively.

1. Introduction

Recently, to reduce the power consumption of the DC source(battery) used in a portable telephone and a mobile communication device (transceiver) as much as possile, a power amplifier with large power added efficiency is required for a transmitter. Such amplifiers have been reported in Refs. [1] and [2]. In the high efficiency power amplifiers described in Ref. [1], the circuit synthesizing the fundamental wave and the third harmonics was used to obtain the voltage waveform which is close to a rectangular form. If we use that waveform, we cannot make the power added efficiency large, and hence the operating angle θ_1 of the synthesized waveform was set to 70° ~74° to have large efficiency. However, the circuit which produces the synthesized waveform was too complicated. To simplify the circuit, we employed a limiter circuit as described in Ref. [2]. When we apply a sinusoidal signal wave to the input terminal of the limiter circuit, this wave is transformed into the trapezoidal wave, which is nearly identical with the synthesized wave used in Ref. [1]. Even when we used this trapezoidal wave, the power added efficiency did not become large unless we set the operating angle θ_1 to 70° ~74° .

In order to increase the power added efficiency using the waveforms in Refs. [1] and [2], we should set the operating angle θ_1 to a value less than 70° . However, for this operating angle, the amplitude of the synthesized wave becomes small and, as a result, the power added efficiency decreases. To increase the efficiency of the amplifier, we need the input power having large amplitude and, hence, we should make the amplification degree large Consequently the consumption of the DC power in the exciting stage increases and the efficiency of the amplifier does not become large.

To solve the problems mentioned above, the author employed a rectangular waveform. Using this waveform, we can change only the operating angle without changing the amplitude of the wave. If the operating angle becomes small, the drain current can flow during the period where the drain voltage is low and, as a result, we can make the power added efficiency high. Considering this advantage, the author constructed a circuit producing a rectangular waveform and also constructed a circuit for keeping its amplitude constant and for making the operating angle small.

2. High Efficiency Single Power Amplifier

This paper describes new high efficiency single amplifier. Fig. 1 shows a circuit system of a high efficiency single power amplifier. In the first circuit for obtaining the rectangular waveform, the amplitude limitation is performed by the circuit of FET1. Through the operation of gate rejection resistor R_2, which is connected to the gate of FET1, the waveform of gate voltage becomes a form shown in Fig. 2. The gate voltage arises from the charge in the capacitor C_1. The time constant τ for charging this capacitor is expressed as

$$\tau = C_1 R_x, \qquad (1)$$

where R_x is given by

$$R_x = R_1(R_2 + R_{gs})/[R_1 + (R_2 + R_{gs})]. \qquad (2)$$

The average value of the gate bias voltage is determined by the gate voltage, and this average value determines the operating point as shown in Fig. 2a. The portion where the gate voltage is positive limits the signal via the voltage decrease $R_2 I_{dd}$. The output waveform arising at the drain side of FET1 is shown in Fig. 2b. The lowest part of the drain voltage corresponds to the period where the gate current flows and, hence, this part is flat because of the amplitude limiting operation of the gate circuit. When the signal voltage of the gate is negative, the drain current deceases and becomes zero at a point where the synthesized voltage of signal and gate voltage reaches the cutoff point.

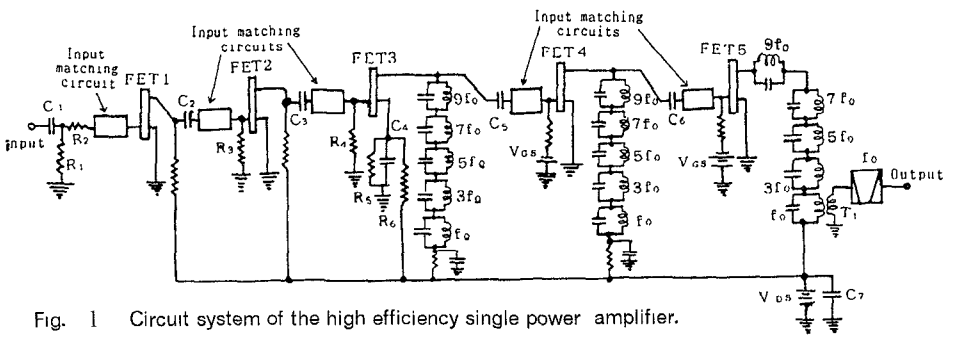

Fig. 1 Circuit system of the high efficiency single power amplifier.

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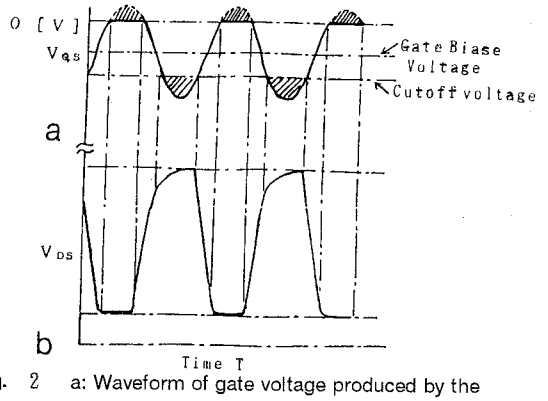

Fig. 2 a: Waveform of gate voltage produced by the rejection circuit. b: Voltage waveform arising at the drain of FET1.

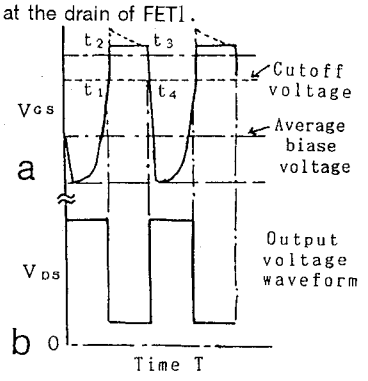

Fig. 3 Voltage waveform produced by the circuit of FET2 shown in Fig. 1.

Since the output volt age shown in Fig. 2b is not perfectly rectangular, this voltage is suplied to the gate of FET2 through the capacitance C_2. The output voltage of FET1 is a pulse with a large amplitude, and the drain current of FET2 is cut at the first part of the negative half period. At the first part of the positive half period, the current reaches the maximum (saturating value). In the positive half period of the output voltage of FET1, a large current flows beween the gate and source of FET2. As a result, the capacitor C_2 is charged and a large negative gate bias voltage is produced. This bias voltage set the reference voltage of the gate to a value below cutoff. As shown in Fig. 3a, the drain current of FET2 does not flow until the input voltage reaches a point t_1 on the curve. At t_1, the drain current of FET2 goes up rapidly and attains a saturaing value at a point t_2. In the time period between t_2 and t_3, the drain current is constant. At t_3, the current goes down rapidly and becomes zero at t_4. Owing to large current flowing between t_2 and t_3, large voltage drop occurs at the drain. As shown in Fig. 3b, large negative voltage is produced across the load at the drain of FET2.

The circuit FET3 in Fig. 1 makes θ_1 small, where θ_1 is the operating angle of the rectangular waveform across the load at the drain of FET2. In order to produce self bias voltage, the parall elcircuit of R_5 and C_4 in FET3 is connected between the source and the earth. If we choose small values for the coupling capacitance C_3 and R_4, the angle θ_1 becomes small. This operation is described in the following.

When the rectangular waveform is supplied to C_3, the differentiated waveform is produced at the gate of FET3 as shown in Fig. 1. By selecting the bias voltage of the gate appropriately, we can obtain the waveform which contains sharp portion of the differentiated waveform. The hatched portion of the waveform in

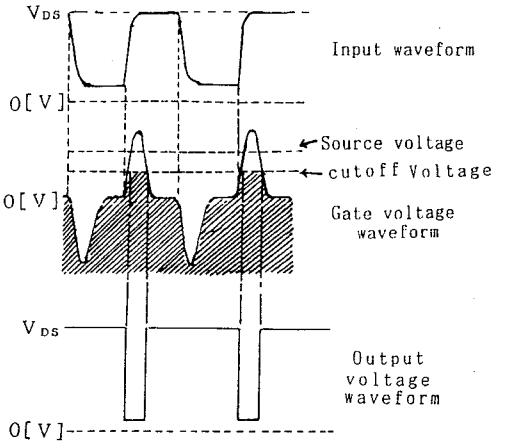

Fig. 4 Input and output waveforms of the circuit of FET3 shown in Fig. 1.

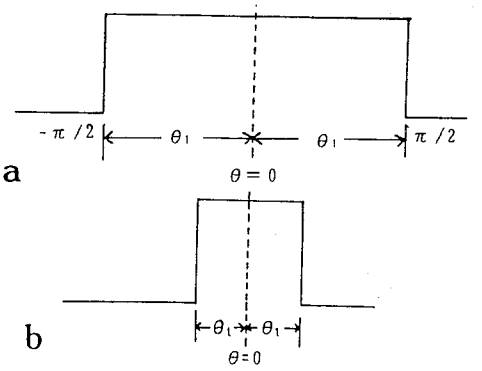

Fig. 5 a: Rectangular waveform for operating angle $\theta_1 = 90°$
b: Rectangular waveform for $\theta_1 = 30°$

Fig. 4 is ineffective and the positive portion which is higher than the cutoff voltage of the gate is effective. Owing to this relatively high voltage, a large drain current flows instantaneously and the negative rectangular waveform is produced because of the voltage drop occuring at the load of the drain. Note that, to eliminate the negative portion of the waveform, the bias voltage of the gate of FET3 should be lower than the cutoff voltage. Accordingly we apply the positive bias voltage to the source through R_5 and R_6, and make the voltage much higher than the earth level. As a result, the negative pulses and wider portions of the positive pulse are eliminated as shown in Fig. 4. When the positive signal is applied to the gate, the gate voltage becomes higher than the source voltage and the rising of the signal is prevented by the amplitude limiting operation of the gate current and the capacitance C_3. Fig. 5a shows the rectangular waveform produced by the circuit of Fig. 1. If we make the values of C_3 and R_4 in the circuit of FET3 small, the operating angle θ_1 of the rectangular waveform becomes small. Figure 5b shows the waveform for $\theta_1 = 30°$.

As described in Refs. [1] and [2], if we make the operating angle θ_1 of the synthesized voltage less than 70°, the amplitude of the voltage becomes small and, owing to this small amplitude, the power added efficiency decreases rather than increases. In order to increase the power added efficiency of the power amplifying circuit, we needed the synthesized voltage with large amplitude and hence it was necessary to make the gain of the exciting stage higher. Consequently, the DC power consumption in the exciting stage became large and we could not improve the efficiency of the power amplifying circuit. On the contrary, if we use the circuit system of Fig. 1, we can change only θ_1 of the rectangular waveform keeping its amplitude constant and do not need to make the gain of

the exciting stage higher. Hence the DC power consumption is small and the waveform shown in Fig. 5 is an ideal one for constructing the high efficiency amplifier.

Now we must transfer thus obtained waveform to the power amplifier in the last stage. To preserve the rectangular waveform at the drain side of FET3, five parallel resonators with resonance frequencies f_0, $3f_0$, $5f_0$, $7f_0$ and $9f_0$ are connected in series and are inserted between the drain of FET3 and the DC source V_{DS}, where f_0 is the resonance frequency of the fundamental wave, and $3f_0$ is that of the third harmonics, etc. The even harmonics are also produced at the drain side of each FET, but since the resonators for these harmonics are not used, they flow through the capacitances of the resonators for odd harmonics. As a result, only the fundamental and odd harmonics exist at the drain side of each FET. Note that, to preserve the waveform of Fig. 5 at the drain side of FET3 by supplying the rectangular waveform to the gate, the odd harmonics up to the 99th harmonics should be included. However, if we use the resonators for these higher-order harmonics, the circuit system becomes large. Hence only five resonators mentioned above were used. When we used these parallel resonators for the fundamental wave to the ninth harmonics, a ripple with small amplitude arose in the top of rectangular wave as shown in Fig. 6, but this ripple did not affect the power added efficiency of the power amplifier.

To construct the resonators, we employed short- circuited $\lambda_g/4$ coaxial-type dielectric resonators. To preserve the rectangular waveform at the drain side of FET3, we must adjust the voltage amplitudes across the terminals of resonators for $3f_0$, $5f_0$, $7f_0$, and $9f_0$ with reference to the voltage amplitude of the fundamental wave. To adjust the voltage, we inserted a conductor into the inner conductor of the coaxial dielectric resonator and changed its depth.

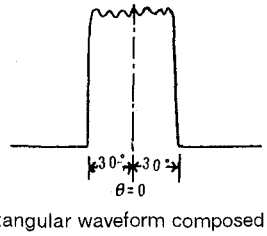

Fig. 6 Rectangular waveform composed of the fundamental wave, the third, fifth, seventh, and ninth harmonics for $\theta_1 = 30°$.

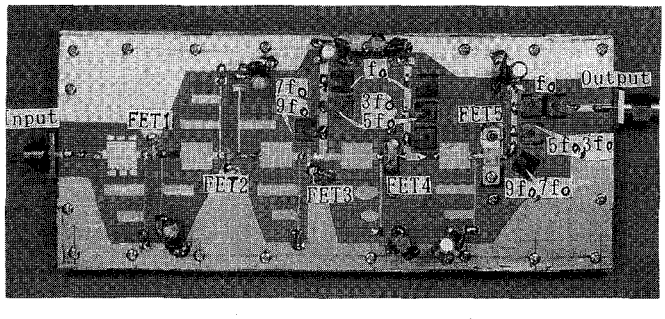

Fig. 7 Photograph of the high efficiency single power amplifier shown in Fig. 1.

The inserted conductor is a cupper wire covered with dielectrics and is led from the transmission line between the drain of FET3 and DC source V_{DS}. By adjusting the depth of the conductor, the coupling is varied and the voltage amplitudes across the resonators are changed. When the coupling is large, the Q-factor Q_L of the parallel resonators is small and the voltage amplitude across the resonators is also small. When the coupling is small, Q_L is large and the voltage amplitude is large. We connected a digitizing oscilloscope to the drain of FET3 and, while observing the waveform, we adjusted the coupling so that the rectangular waveform was obtained. If we construct the five resonators by microstrip lines, it is difficult to adjust the voltage amplitude of each resonator. On the contrary, if we use the coaxial-type resonators, it is easy to adjust the voltage amplitude by changing the coupling.

The rectangular output from FET3 is amplified at the exciting stage of FET4, and its power is amplified by the power amplifier in the last stage of FET5. Five parallel resonators with resonance frequencies f_0, $3f_0$, $5f_0$, $7f_0$, and $9f_0$ are connected in series and inserted between the drain and DC source V_{DS} to preserve the rectangular waveform at the exciting stage of FET4 and at the drain side of the power amplifier of FET5. By using rectangular waveform, the time period when the current flows becomes short and therefore the power added efficiency becomes large. The use of coaxial-type dielectric resonators makes the Q-factor of the parallel resonator large, and as a result, we can obtain the large output from the power amplifier. The power-amplified output is taken out from the secondary side (T_1) of the resonator for the fundamental wave. Since this output contains higher-order harmonics, a band-pass filter for f_0 is connected.

3. Experimental Results

Figure 7 shows a photograph of the circuit system of Fig. 1. The measurement was performed on the high efficiency power amplifier shown in this photograph. The voltage V_{DS} applied between the drain and source of FET5 is 10 V, and the bias

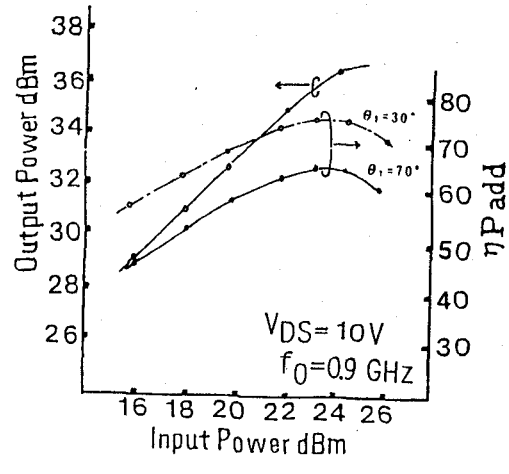

Fig. 8 Dependence of the output power and the power added efficiency on the input power for the amplifier of Fig. 7.

volatage V_{GS} applied between the gate and source is -3.6 V. This bias voltage is set at the cutoff point V_p and the amplifier works as a class B power amplifier. For constant input power of 22 dBm and for the operating angle of 70°, the frequency was varied from 0.7 to 1 GHz and we obtained the output power 35 dBm, the bandwidth 40 MHz, and the power added efficiency 65 %. When the input power was varied from 16 to 25 dBm, the output power changed from 28.4 to 36.4 dBm and the power added efficiency changed from 28.2 to 65 %. The measured frequency, characteristics are shown in Fig. 8. In addition, when we set θ_1 to 30° by decreasing the values of capacitance C_3 and resistance R_6, we obtained the power added efficiency 76 %.

Figure 9 shows the measured results of the input-output characteristics and third order intermodulation distortion of the power amplifier. The measurement was done with a spectrum

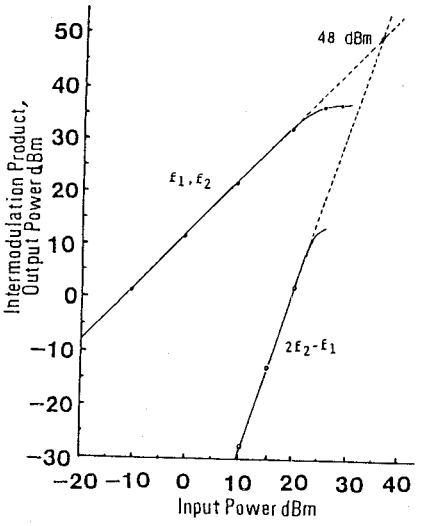

Fig. 9 Output power and third order intermodulation production versus input power at the center frequency (f_1 =0.9GHz, f_2 =0.905GHz)

analyzer by injecting into the amplifier the fundamental signal at 0.9 GHz and the signal with the same level but at frequency shifted by 5 MHz. The intercept point was 48 dBm.

4. Conclusion

This paper described a new high efficiency single power amplifier. As stated in Refs. [1] and [2], the most important point in constructing the high efficiency power amplifier is to synthesize the waveform for which the current flows during the period when the DC voltage is low. However, the waveform used in these references was trapezoidal one. In this case, even if we want to increase the power added efficiency by making the operating angle θ_1 less than 70°, the voltage amplitude becomes small and the power gain at the exciting stage decreases and we cannot obtain a high value of the power added efficiency at the last stage. Hence, in this paper, we used the rectangular waveform. In this case, we obtained the power added efficiency 76% by setting its amplitude constant and by making the operating angle θ_1 small. Further, it was confirmed by the experiment that the large output power is obtained and the DC power consumption is small if we use the parallel resonators with high Qu and the FET with small output power.

References

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